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Ultrathin tin sulfide field-effect transistors with subthreshold slope below 60 mV/decade

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Abstract

In this paper, we present for the first time a field-effect-transistor (FET) having a 10 nm thick tin sulfide (SnS) channel fabricated at the wafer scale with high reproducibility. SnS-based FETs are in on-state for increasing positive back-gate voltages up to 6 V, whereas the off-state is attained for negative back-gate voltages not exceeding −6 V, the on/off ratio being in the range 10^2–10^3 depending on FET dimensions. The SnS FETs show a subthreshold slope (SS) below 60 mV/decade thanks to the in-plane ferroelectricity of SnS and attaining a minimum value SS = 21 mV/decade. Moreover, the low SS values can be explained by the existence of a negative value of the capacitance of the SnS thin film up to 10 GHz (for any DC bias voltage between 1 and 5 V), with the minimum value being −12.87 pF at 0.1 GHz.

Keywords: 2D materials ferroelectricity, ferroelectrics, microwaves, RF magnetron sputtering, semiconductors, thin films, tin sulfide

(Some figures may appear in colour only in the online journal)

1. Introduction

Tin sulfide (SnS) is a non-toxic, earth-abundant direct band-gap semiconductor (bandgap $E_g = 1.3$ eV), used in many photonic and electronic applications, such as photodetectors, solar cells, photochemical cells, battery anodes, and gas sensors [1, 2]. SnS is a van der Waals material formed by piled-up monolayers [3] in a way similar to graphite, which is formed by many graphene monolayers. Moreover, ultrathin SnS exhibits giant piezoelectric coefficients [4].

The discovery of 2D materials triggered new research about atomically-thin SnS having a thickness ranging from a Sn–S double atomic monolayer up to few double atomic layers, but not exceeding 10–15 nm. In these ultrathin SnS films a pure in-plane ferroelectricity emerges [4], and SnS films with a few-atom thickness have found applications in ferroelectric analogue synaptic devices for artificial neural network applications [5], and nonlinear optics [6]. Very recently, the microwave properties of a 10 nm thick SnS

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film grown on a silicon dioxide/high-resistivity silicon (SiO_2/HRSi) 4 inch wafer by RF magnetron sputtering [7] have been presented. Gold coplanar waveguides (CPWs) were deposited over the SnS thin layer to excite an in-plane electric field able to tune and switch the in-plane polarization of the SnS; as a result, it was observed that the considered 10 nm thick SnS film exhibits excellent microwave performance. Since the ultrathin SnS is ferroelectric, it can be also used in a straightforward way for miniaturized microwave phase shifters and, in our case, it was obtained a phase shift of 30 degrees·mm^{-1} at 1 GHz and of 8 degrees·mm^{-1} at 10 GHz, whereas the transmission losses were less than 2 dB in the frequency range 2–20 GHz. In addition, it was experimentally evidenced that SnS is a microwave detector, which provides a voltage responsivity of about 30 mV·mW^{-1} at 1 GHz in the unbiased case, with an input power level of only 16 μW, thus able to harvest the ambient electromagnetic energy.

Another way to generate in-plane electrical fields (i.e. in parallel with the in-plane polarization of the ferroelectric layer) is to use ultrathin films of SnS as transistor channel, the drain-source voltage being the origin of this parallel electric field able to control and switch the in-plane polarization of SnS dipoles. There are few reports about SnS field-effect-transistors (FETs), all being fabricated on SnS flakes with no reproducibility tests whatsoever. These SnS-based devices were used to test the in-plane ferroelectricity, but no performances or targeted applications were envisaged [8].

Therefore, it was necessary to identify a technological process to fabricate SnS FETs at the wafer scale and suitable to provide tens of FETs with comparable performance. Since the majority of atomically thin ferroelectrics are semiconductors detached from their parent materials [9, 10], the role of this manuscript is to propose atomically thin SnS as an ultrathin ferroelectric material grown at the wafer scale and having similar applications as the wafer-scale semiconductor ferroelectrics AlScN [11] or the HfO_2-based ferroelectrics [12].

2. Characterization and fabrication of the SnS transistors

The SnS thin films were grown with the same method and characterized (including their ferroelectricity nature) in the same way as reported in [7]; hence, these results will not be repeated here. Ultrathin layers of SnS have been deposited on two Si wafers by RF magnetron sputtering techniques. Each wafer has a diameter of 2 inch and the SnS was deposited on 50 nm thick SiO_2, which was thermally grown on doped Si. The thickness of the film was measured during the deposition process using a quartz sensor with standardized coefficient from Tectra GmbH Thickness Monitor, which can measure the thickness with a precision of $\pm$0.1 nm. Then, we fabricated SnS-based transistors having as back-gate the doped Si substrate (figure 1(a)), thus allowing the control of the drain current in the SnS channel. The SnS channel was fabricated with various widths W (i.e. 0.5, 1, 2, and 5 μm) and various lengths L (0.5, 1, 2, and 5 μm). The SnS-based transistors were fabricated on the same wafer using various combinations between the width and length values.

The fabrication process consists in several steps. The first step encompasses the register marks fabrication, thus implying patterning, metal deposition, and lift-off. We designed four marks placed in the corners of an 80-μm-wide square (figure 1(b)) to perform the overlay in the further steps. These marks were patterned in 950k A4 PMMA spun at 1500 rpm and exposed at 30 kV. All patterning steps were performed using a Raith e-Line electron beam (e-beam) lithography (EBL) system and all metallic layers were deposited using a Temescal FC2000 e-beam evaporator. For these marks, 5 nm of Ti and 100 nm of Au were deposited. The lift-off process was performed in acetone for a few hours. The second step was dedicated to the SnS channel fabrication. For the etching of the SnS layer, the SnS sample was coated with PMMA, exposed, and developed. Then, the etching was performed by reactive ion etching (RIE) method. Finally, the PMMA was removed in acetone. The area of the SnS channel was surrounded by a large (i.e. 500 μm $\times$ 300 μm) empty space dedicated to the electrical pads (figure 1(c)).

Since the etching process for ultrathin SnS channels is still unknown, we provide in the following a detailed description. The etching of the SnS thin films was performed using the Etchlab SI220 (Sentech Instruments, Germany), a plane parallel capacitively coupled RIE system. The preferred etching method was physical etching, achieved by using an Argon plasma (Ar gas, purity 99.999% supplied by Linde Gas). The etching process was carried out at a pressure of 2 Pa (i.e. 15 mTorr), while the plasma was ignited and maintained by applying a 350 W RF power to the lower electrode. The etch rate of the masking PMMA layer was determined to be approximately 6.5 nm s^{-1} by measuring the resist thickness using the Nano-Calc-XR reflectometer (OceanOptics, USA) before and after plasma exposure. For completely etching of the SnS thin films, a total exposure time of 20 s was determined to be the optimal choice. The third step was represented by the fabrication of the source and drain contacts. The SnS wafer was coated again with PMMA 950k A4, exposed at 30 kV and 300 μC cm^{-2}, and developed. Then, 5 nm of Ti and 100 nm of Au were evaporated (figure 1(d)). One of the processed SnS wafers and the fabricated SnS FETs are displayed in figure 2.

3. Electrical characterization and discussions

The electrical characterization of the SnS FETs was performed on-wafer by means of a Keithley SCS 4200 station. The probe station for on-chip measurements is located inside a Faraday cage and its cables are connected to the station via low-noise amplifiers. No fitting algorithms were used during or after measurements. All transistors existing on two identical wafers and fabricated with the same technological processes were measured. All measurements were performed at room temperature. The fabrication yield was around 80%, hence very high considering that these types of FETs have been never fabricated before. The exfoliation of the metallic contacts due to the pressure of the probe tips during DC

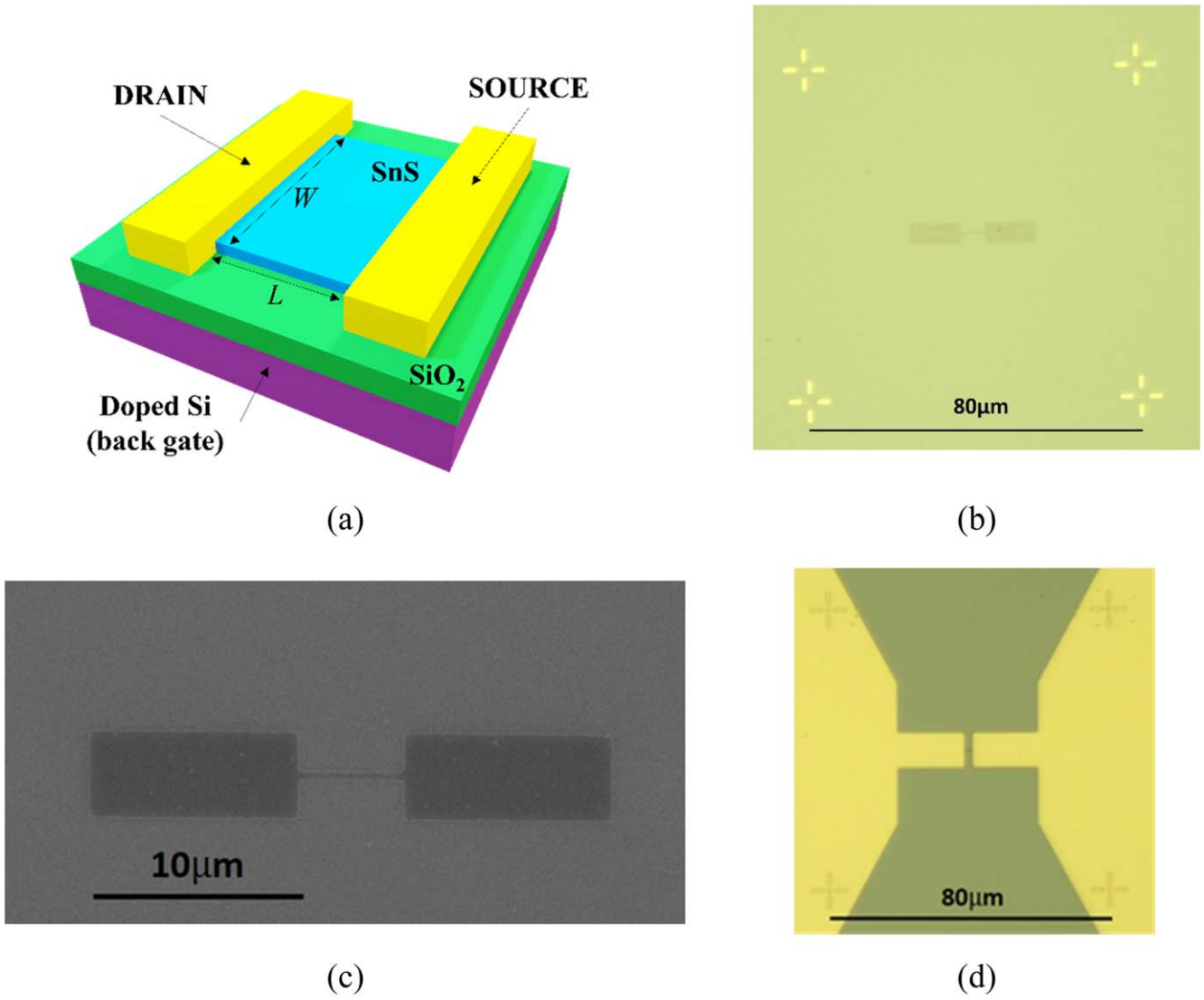

Figure 1. (a) 3D schematic of the SnS-based FET; scanning electron microscope (SEM) and optical images of the (b) register marks, (c) SnS channel, and (d) source and drain contacts for the fabrication of the SnS-based FETs.

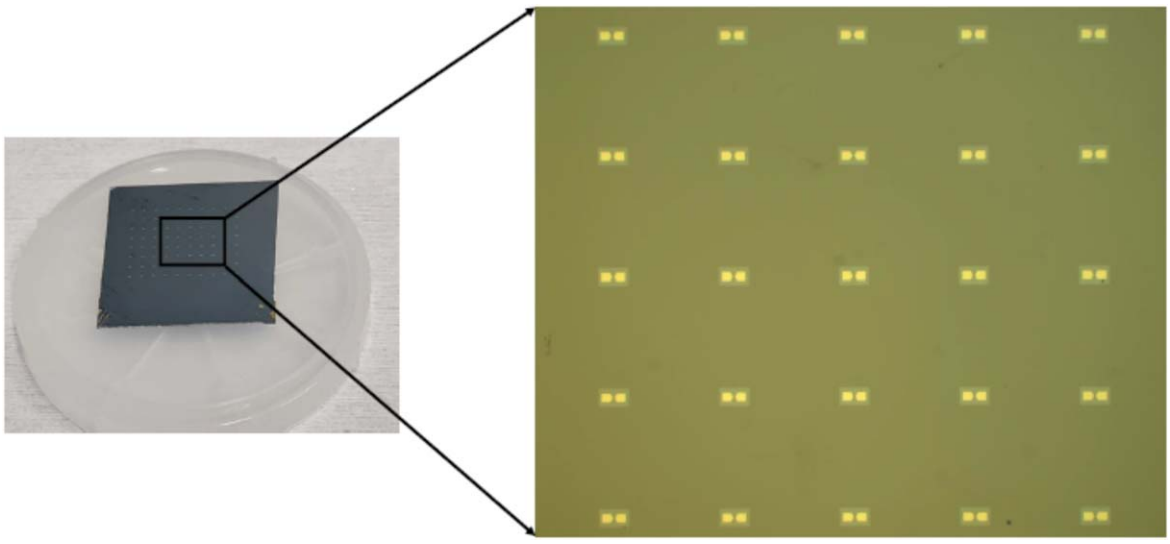

Figure 2. (Left) One of the processed SnS wafers and (right) a magnification with the fabricated SnS-based FETs.

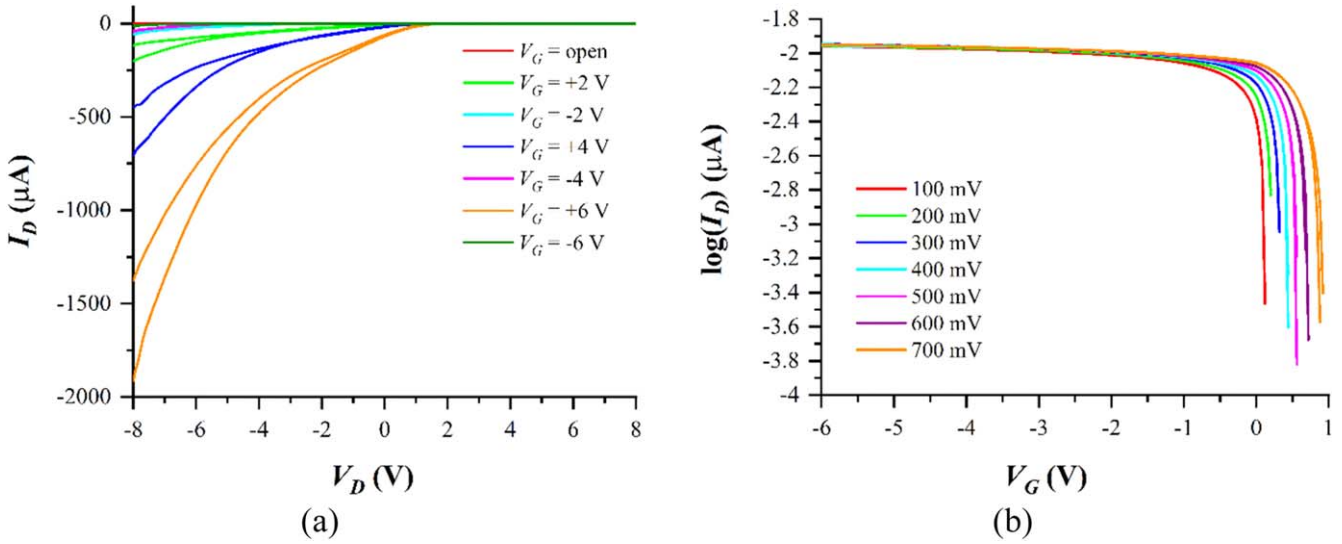

Figure 3. *I–V* characteristics for the SnS FETs with $W = 2$ μm and $L = 0.5$ μm: (a) I_D–V_D dependence at different V_G values; (b) log (I_D)–V_G dependence at different low V_D values.

measurements was the main cause of defects for the proposed devices. As stated in section 2, on each wafer SnS FETs with various width W and length L values were fabricated (W, $L = 0.5$, 1, 2, and 5 μm). Each one of the 16 possible combinations was fabricated 5 times, meaning that each SnS wafer contains 80 FETs. Hence, the total number of measured devices was 160. We will present in the following a synthesis of these experimental results made on the two wafers.

The drain current (I_D) dependence on the drain voltage (V_D) at different back-gate voltage values (V_G) is represented in figure 3(a) in the case when the width and length of the SnS FETs channel are $W = 2$ μm and $L = 0.5$ μm, respectively. Ten identical transistors were measured with similar results. The hysteretic nature of the I_D–V_D characteristic reflects the parallel ferroelectric polarization of the SnS. In the same way, for vertically polarized ferroelectrics the I_D–V_D curve is hysteretic and reflects the intrinsic memory effect of vertically polarized ferroelectrics. We can observe that $I_D = 2$ mA for $V_D = -8$ V and $V_G = 6$ V, this value of I_D being very high for such channel dimensions. Therefore, we did not increase $|V_D|$ over 8 V, which explains why the hysteretic curves are not closed, since a further increase of V_D could destroy the thin channel knowing that the coercive voltage is around 10 V [7]. Moreover, all the hysteretic dependences are in the clockwise direction. Finally, the log(I_D)–V_G characteristics at different low V_D values are displayed in figure 3(b). We have measured the I_D–V_G dependence with V_G spanning between -6 V and 6 V; however, in figure 3(b) we have used the range $[-6, 1]$ V for V_G to better illustrate the abrupt decay of the drain current.

From figure 3(b) one can see that we have an on/off ratio of 10^2 at $V_D = 500$ mV and a subthreshold slope or swing SS $= \partial V_G/(\log I_D)$ of 43 mV/decade in the abrupt region of the I_D–V_G characteristics, which is below the 60 mV/decade for CMOS transistors. In this case, no significant hysteresis can be observed, the hysteresis width being $\Delta V_G = 20$ mV. This negligible value could be explained by the fact that in the case of in-plane polarized ferroelectric FETs, the gate changes only the drain current, thus not playing any role in the ferroelectric switching. Moreover, the remanent polarization of SnS thin films is 40 μC cm^{-2} (like in HfO_2-based ferroelectrics) and the coercive field is three orders of magnitude lower (i.e. around 60 kV cm^{-1} [5]); hence, the density of charges involved in the hysteretic process is much more reduced.

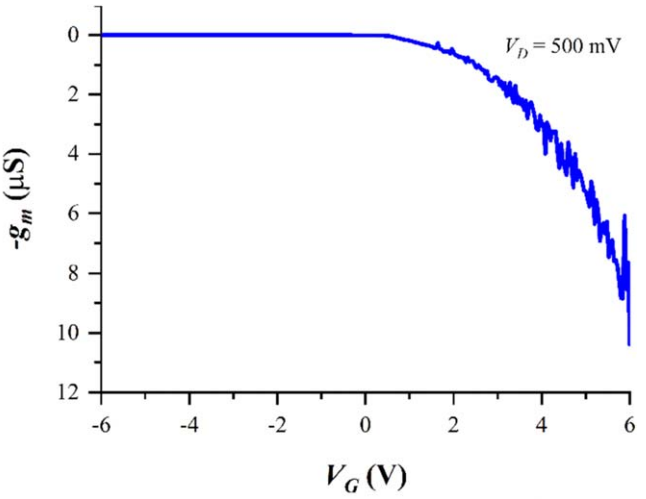

Figure 4. Transconductance g_m of the SnS FET $W = 2$ μm and $L = 0.5$ μm at $V_D = 500$ mV.

We stress here that the current-voltage dependence does not cross the zero point because SnS is a ferroelectric, therefore there is a built-in electric field inside it in the absence of any external applied voltage. This effect is equivalent to the existence of a remanent polarization in any ferroelectric. In figure 4 we show the calculated transconductance g_m (at $V_D = 500$ mV), which is equal to 10 μS for $V_G = 6$ V.

To achieve SS values below 60 mV/decade is a hot topic, since it has great implications in the reduction of the power consumption of the transistors (for a review see [13] and [14]). For example, 2D semiconductor materials like MoS_2 deposited over CMOS-compatible ferroelectrics such

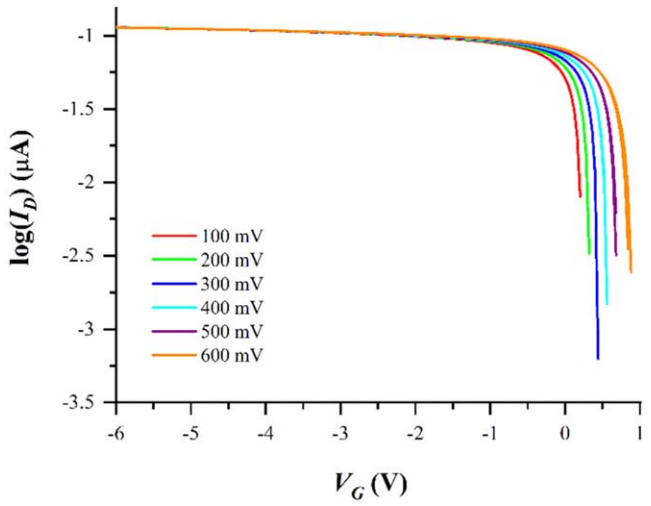

Figure 5. log(I_D)–V_G dependence at different V_D values when $W = 1$ μm and $L = 2$ μm.

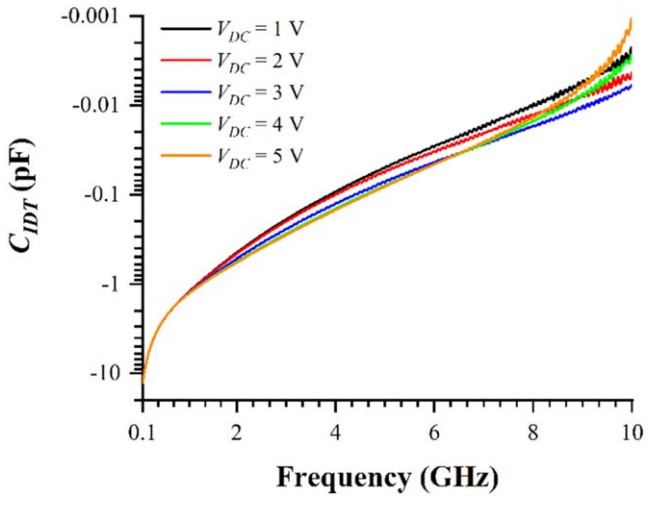

Figure 6. Microwave capacitance C_{IDT} of the SnS-based IDTs, in the frequency range 0.1–10 GHz, for different values of the DC bias voltage V_{DC} (between 1 and 5 V).

as hafnium oxide doped with zirconium (HfZrO, [15]) or integrated with $CuInP_2S_6$ (CIPS) [16] have shown SS values well below 60 mV/decade thanks to the negative ferroelectric capacitance. Therefore, we tested other transistors with other channel dimensions to verify if a SS value below 60 mV/decade could be preserved. In this respect, we measured SnS FETs with a decreased width and an increased length, i.e. $W = 1$ μm and $L = 2$ μm. The I_D–V_D characteristics at different values of V_G are similar to the ones shown in figure 3(a), with I_D decreasing to 1.6 mA for $V_D = -8$ V and $V_G = 6$ V. However, the I_D–V_G dependence is improved (figure 5): since it becomes more abrupt at increasing V_G, the transconductance is increased at 26 μS, and for $V_D = 300$ mV we have SS = 21 mV/dec, with $\Delta V_G = 9$ mV and the on/off ratio around 10^3. The measurements were performed on 10 transistors with similar results.

Decreasing the SnS channel dimensions to $W = 0.5$ μm and $L = 0.5$ μm does not improve the SS, which reaches the lowest value of 64 mV/decade at $V_D = 200$ mV. Also in this case, ten different transistors were tested. Others SnS-based FETs were tested with similar results, i.e. with SS in the range between 50 and 60 mV/decade.

Transistors having low SS values are based on specific physical phenomena [13], e.g. tunneling, impact ionization, cold-sources, and negative capacitance FETs due to the negative capacitance of ferroelectrics. We believe that this last effect is at the origin of the low SS values in SnS-based FETs, but the negative capacitance in the case of parallel polarized ferroelectrics is completely unstudied, this situation being in deep contrast with ferroelectrics with vertical polarization where tens of papers and reviews can be found in the literature [17–19]. To tackle this issue in the present case of study, we fabricated interdigitated capacitors (IDTs) in CPW technology directly on a SnS thin film on a SiO_2/HRSi wafer, as done in [7], with the same process and thickness as the channel of the SnS FETs considered here; then, we characterized these IDTs at microwaves. An IDT consists of 250 digits, a single digit having a length of 100 μm, a width of 250 nm, and the gap between two consecutive digits being 200 nm. The IDT is embedded into a CPW line having the length of the central conductor of 100 μm and a gap of 60 μm between the central conductor and each one of the lateral ground electrodes. This guarantees a characteristic impedance of 50 Ω of the CPW line, which can be measured on-wafer in a straightforward way by using a vector network analyser. As displayed in figure 6, the measured microwave capacitance C_{IDT} is negative at any applied DC voltage (up to 5 V) over a wide range of frequencies spanning between 0.1 and 10 GHz. In detail, if we define V_{DC} as the DC bias voltage, S_{11} as the reflection coefficient at port 1 of the generic IDT structure, f as the frequency, and Z_0 as the characteristic impedance of the CPW line, then we can use the following equation to extract IDT's capacitance from the measured scattering parameters:

$$C_{IDT}(V_{DC}) = -Im\{S_{11}(V_{DC})\}/\{\pi f Z_0[(1 + Re\{S_{11}(V_{DC})\})^2 + Im\{S_{11}(V_{DC})\}^2]\}. \quad (1)$$

Using equation (1), we verified that C_{IDT} is always positive in the unbiased case (with values attaining the range between 0.01 and 1.78 pF), whereas biasing the SnS layer allowed obtaining negative values of C_{IDT} (the minimum value being −12.87 pF at 0.1 GHz) up to 10 GHz (for any V_{DC} between 1 and 5 V). The explanation of such results could be the intrinsic nature of the microwave components (i.e. CPW-based IDTs) used for the experiments, suitable for the application of a horizontal DC bias voltage, thus in parallel with the in-plane polarization of the ferroelectric SnS layer.

4. Conclusions

In this paper, we have presented for the first time the fabrication (at the wafer scale) of tens of transistors having an ultrathin film of SnS as channel. These SnS-based FETs exhibit SS values below 60 mV/decade as many other ferroelectric transistors

with vertical electrical polarization. However, in all vertically polarized ferroelectric FETs the channel of the transistor is a distinct material and is located above or below the ferroelectric, which is an insulator. In deep contrast with the latter situation, in the proposed solution the ultrathin SnS with parallel electric polarization is both the channel and the ferroelectric. The investigation of the negative capacitance in the case of parallel electric polarization ferroelectrics is a non-trivial topic, which will be the object of further research in a future paper.

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Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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